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EXAMINER	
LANGMAN, JONATHAN C	

ART UNIT	PAPER NUMBER
1794	

NOTIFICATION DATE	DELIVERY MODE
10/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/539,260	HAISMA, JAN	
	Examiner	Art Unit	
	JONATHAN C. LANGMAN	1794	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicant is supported for the oxidation of a carrier material when the carrier material is a semiconductor (see paragraph [0031]) of the PG Publication. .However the applicant is not supported for the entire range of all oxides of carrier materials, but only supported for oxides of semiconductor carrier materials.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what the applicant means by the statement that the locations are where stress is likely to occur. Does stress necessarily have to occur? Will stress incur over the entire substrate? The applicant is attempting to define a

location of the intermediate structures by using an indefinite description. It is unclear as to where these structures will be located in the structure. Clarification is needed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 and 21-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation.

In regards to claims 1, 4, and 5, the applicant is essentially claiming a bonded wafer comprising two substrates (a carrier and a first layer) wherein the two substrates are separated by an intermediate layer (insulator), wherein the insulator has structures. Any SOI bonded wafer in the art would read on this claim, and if the insulator layer is patterned then it would read on all the instant dependent claims instantly set forth. Haberger et al. teach an SOI wafer comprising a first substrate and a second substrate bonded to each other by their faces via one or several intermediate bonding layers. At

least one of the bonding layers is configured that it presents channel shaped recesses (col. 3, lines 62-66). The two substrates are preferably semiconductor substrates (col. 4, lines 5), and specifically mention the substrates to be silicon (see the entire specification). Two silicon wafers will have dilatation behaviors that are substantially the same, since they are the same material. The bonding layers are taught to be SiO_2 in preferred embodiments (col. 5, lines 1-8). A SiO_2 layer has a dilatation mismatch with the first layer (silicon). The patterned trenches are structures that expectantly and inherently absorb stress originating from the dilatation mismatch.

Regarding claims 2 and 3, the insulator (bonding) layers are taught to be buried oxide layers (col. 4, line 66), thus showing that the structures comprised of the insulating material further extend into the carrier. The trenches are formed of the same material and by the same process as instantly claimed (selective patterning with photolithography and then wet or dry etching), and therefore are expected to have the same structural features as instantly claimed.

Regarding claim 6, SiO_2 is electrically insulating.

Regarding claim 7, Haberger et al. teaches that the width of the trenches and height of the trenches is less than one centimeter (col. 6, lines 61-64).

Regarding claim 8, the channels have a linear orientation perpendicular to a plane of the carrier (col. 4, lines 38-39, and figures 2).

Regarding claim 9, the channels are rectangular in shape and extend across the wafer (figure 2), therefore, the structures are parallel to a plane of the carrier. Furthermore, Haberger et al. describe that the structures need not present a rectangular

cross section, or across linear orientations (col. 4, lines 38-43), therefore the channels may take on any shape desired, including those instantly claimed.

Regarding claim 10, the composite substrate is an SOI wafer.

Regarding claim 21, the layers are all bonded to each other (col. 3, lines 60-65).

Regarding claim 22, the wafers of Haberger et al are silicon and the intermediate layer is silicon oxide (see at least (col. 5, lines 1-5, and col. 2, lines 25-35).

Regarding claim 23, buried oxide layers are taught (col. 2, lines 25-35).

Regarding claim 24, Haberger teaches rounded corners (col. 4, lines 40-53).

Regarding claims 25-27, the structure of Haberger is the same as instantly claimed, and Haberger teaches placing the structures at selected locations of the intermediate layer (see the figures). For these reasons it is the examiner's position that since Haberger teaches the same materials, the same structures, and the same spacing, that they will inherently and expectedly possess the same characteristics of stress relief as instantly claimed, and removing dislocations as instantly claimed. Stress is expected to occur between the mismatched layers, and since Haberger teaches the same structures as instantly claimed and the same position of the intermediate layer as instantly claimed, the structures of Haberger are said to be located at least where there is some degree of stress originating from the dilatation mismatch. It has been held that where the claimed and prior art products are identical or substantially identical in structure or are produced by identical or a substantially identical processes, a prima facie case of either anticipation or obviousness will be considered to have been established over functional limitations that stem from the claimed structure. *In re Best*,

195 USPQ 430, 433 (CCPA 1977), *In re Spada,* 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). The ***prima facie*** case can be rebutted by evidence showing that the prior art products do not necessarily posses the characteristics of the claimed products. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 28, the structure of Haberger is in the shape of free standing elongated pillars on the carrier layer (see the figures).

Claims 1, 2, and 4-10, 21, 22, and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Schrantz et al. (US 5,552,345).

Regarding claims 1, 2, 4-6, 8-10, 21, and 22, Schrantz et al. teach a silicon on insulator substrate wherein diamond is the insulator. As seen in Figures 2a-2b, a bonded structure comprising a silicon wafer 2, diamond layer 3 and device layer, 4, (silicon per col. 3, lines 43) is shown. The diamond insulator layer is patterned and portions of it are selectively removed in order to define a series of scribe lines 6 (col. 4, lines 37-52). The streets, 6, may be left void (col. 4, line 26). The term series" of "scribe lines" also seen in figures 2a-2c denotes a linear formation, thus reading on instant claim 8, and the rectangular shape of instant claim 9. The two silicon wafers, 2 and 4 have the same dilation behavior, and diamond has a different dilatation behavior than that of the carrier. The diamond layer is formed into structures by patterning and etching, therefore showing that the structures extend through the thickness of the diamond layer, and will inherently and expectantly absorb stress originating from the dilatation mismatch.

Regarding claims 1, 2, 4-10, 21,and 22, Schrantz further teach another embodiment taught that reads upon the applicants instantly claimed structure; this structure is shown in Figures 4, specifically, figures 4c-4e, wherein 4e omits the sacrificial silicon wafer, 2, bonded to the bottom of layer 3. This structure comprises sacrificial wafer, 2, not shown, SiO_2, insulating materials 26, patterned and distributed between the handle wafer and the device wafer 20, which also comprises silicon. The patterned SiO_2 material 26, will inherently and expectantly absorb the dilation mismatch between the device layer, 20, and the handle layer 2, or as a matter of fact any layer disposed there under. The SiO_2 layers have lateral size of 2-5 microns (col. 6, lines 4-24) and are in the shape of squares (fig. 4c) thus reading on instant claim 9. A square also is in the shape of a short line, thus reading on instant claim 8. Schrantz et al. teach that the sacrificial layer is removed, however this occurs after bonding. Therefore the instantly claimed structure is realized after bonding but before the removal of the sacrificial layer 2.

Regarding the orientation limitations of claims 8 and 9; by the applicant describing the structures as lying perpendicular or parallel to **"a plane"** is irrelevant because the applicant has not defined these carrier planes, and therefore any structure on the surface of the carrier will be said to be lying perpendicular or parallel to any plane of the carrier material. As seen in figures 4, the structure has the shape of a pillar.

Regarding claims 25-27, the structure of Schrantz is the same as instantly claimed, and Schrantz teaches placing the structures at selected locations of the intermediate layer (see the figures). For these reasons it is the examiner's position that

since Schrantz teaches the same materials, the same structures, and the same spacing, that they will inherently and expectedly possess the same characteristics of stress relief as instantly claimed, and removing dislocations as instantly claimed. Stress is expected to occur between the mismatched layers, and since Schrantz teaches the same structures as instantly claimed and the same position of the intermediate layer as instantly claimed, the structures of Schrantz are said to be located at least where there is some degree of stress originating from the dilatation mismatch. It has been held that where the claimed and prior art products are identical or substantially identical in structure or are produced by identical or a substantially identical processes, a prima facie case of either anticipation or obviousness will be considered to have been established over functional limitations that stem from the claimed structure. *In re Best*, 195 USPQ 430, 433 (CCPA 1977), *In re Spada,* 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). The ***prima facie*** case can be rebutted by evidence showing that the prior art products do not necessarily posses the characteristics of the claimed products. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Claims 1, 2, 4-6 and 9-10, 21, 22, 25-27, and 28 are rejected under 35 U.S.C. 102(a) and 102 (e) as being anticipated by Chong et al. (US 6,544,863).

Chong et al. teach in Fig 2d, the instantly claimed structure. A substrate 201 that may be a semiconductor or silicon is covered with a layer of silicon dioxide 202, (an insulator). A stencil of the desired pattern may then be placed upon the insulating layer 202 to provide a patterned insulating layer on the silicon substrate 201. A substrate material 203, which is of the same material as the silicon layer 201, is then bonded to

the patterned side of the protective layer (col. 3, lines 50-67). The patterned structures of the silicon oxide layer expectantly and inherently absorb the dilation mismatch between the semiconductor substrates and the intermediate film, silicon dioxide.

Regarding claims 9 and 28, as seen in figures 2c and 2d, the silicon oxide has a rectangular shape parallel to a plane of the carrier, a rectangular shape takes on the shape of a wide pillar.

Regarding claims 25-27, the structure of Chong is the same as instantly claimed, and Chong teaches placing the structures at selected locations of the intermediate layer (see the figures). For these reasons it is the examiner's position that since Chong teaches the same materials, the same structures, and the same spacing, that they will inherently and expectedly possess the same characteristics of stress relief as instantly claimed, and removing dislocations as instantly claimed. Stress is expected to occur between the mismatched layers, and since Chong teaches the same structures as instantly claimed and the same position of the intermediate layer as instantly claimed, the structures of Chong are said to be located at least where there is some degree of stress originating from the dilatation mismatch. It has been held that where the claimed and prior art products are identical or substantially identical in structure or are produced by identical or a substantially identical processes, a prima facie case of either anticipation or obviousness will be considered to have been established over functional limitations that stem from the claimed structure. *In re Best*, 195 USPQ 430, 433 (CCPA 1977), *In re Spada,* 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). The ***prima facie*** case can be rebutted by evidence showing that the prior art products do not necessarily

posses the characteristics of the claimed products. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being anticipated by Haberger et al. (WO9967820), published December 29, 1999, whose US counterpart (US 6,417,075), is referenced as the English translation, as applied above.

Haberger et al. teach a SOI substrate comprising two semiconductor wafers separated by a patterned oxide insulating layer of silicon dioxide, as described above. Haberger et al. teach shapes and sizes as seen in figures 2 and 3, and mentioned above, but do not teach all of the shapes instantly claimed. However, it would have been obvious to a person having ordinary skill in the art at the time the present invention was made, and well within their grasp, to choose any desired pattern including those shapes and sizes instantly claimed, as these are shown to be desired effective results. It would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the shapes and sizes of patterns in the insulating layer for the intended application, since it has been held that discovering an optimum value of a

result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 3, 7-9, 23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (US 6,544,863), as applied above.

Regarding claims 3 and 23, Chong et al. teach a SOI substrate comprising two semiconductor wafers separated by a patterned oxide insulating layer of silicon dioxide, as described above. Chong et al. is silent to the structures of the oxide layer extending into the handle wafer, however, buried oxide layers are well known in the art and obvious for using in SOI wafers. If a buried oxide insulating layer is used, and subsequently patterned by the methods of Chong et al., the structures would then extend into the handle or carrier substrate.

In regards to claims 7-9, Chong et al. teach that the insulating layer may be patterned as desired. It would have been obvious to a person having ordinary skill in the art at the time the present invention was made and well within their grasps to choose any desired pattern including those shapes and sizes instantly claimed, as these are shown to be desired effective results. It would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the shapes and sizes of patterns in the insulating layer for the intended application, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

Applicant's arguments filed June 18, 2008 have been fully considered but they are not persuasive.

The applicants' argue that the Haberger reference discloses slots in a sacrificial bonding layer that are provided for the supply and extraction of an etchant and that because the slots are part of a sacrificial layer they are no longer present after processing. It is the examiners position that the bonded structure before processing realizes the instantly claimed structure. The applicant argues that Haberger is not related to the use of the intermediate layer structures for the relief of stresses caused by dilatation mismatch with the material of the intermediate layer. It is the Examiner's position that since Haberger teaches the same structure, including a handle wafer, a device wafer and an intermediate bonding layer including "structures" thereon, that the structure will inherently and expectedly possess the claimed stress relief. It has been held that where the claimed and prior art products are identical or substantially identical in structure or are produced by identical or a substantially identical processes, a prima facie case of either anticipation or obviousness will be considered to have been established over functional limitations that stem from the claimed structure. *In re Best*, 195 USPQ 430, 433 (CCPA 1977), *In re Spada*, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). The ***prima facie*** case can be rebutted by evidence showing that the prior art products do not necessarily posses the characteristics of the claimed products. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

This same rationale is applied to the applicant's arguments in regards to both Schrantz and Chong. The intermediate products, before processing of these references is identical to the instantly claimed article. It is expected and inherent that since they both teach the same structure that the structure will act in the same way as instantly claimed, specifically relieving the stresses between the dilatation mismatch between the substrates and the intermediate layer.

The applicant has not shown or argued persuasively that the structures of Chong, Schrantz, and Haberger et al. do not provide stress relief. It is the examiner's position that because these references are silent to the stress relief does not mean that the stress relief is not present in Haberger, Schrantz, and Chong.

The applicant argues that the stress relief is not inherent in Chong, Schrantz and Haberger because for a property to be inherently it must be necessarily flow from a claimed structure. It is the Examiner's position that since the references teach the same structure than they will have the same properties as instantly claimed. See the In Re Best case law presented above. Therefore, the examiner has provided a basis for the conclusion of inherency.

The applicant further argues that the applicant's specification discusses various dimensions, extensions, provision of rounded corners and particular structures, and that the stress relief is not inherent in such cited references where the dimensions and geometries do not allow stress induced dislocations in a structure to migrate to a free surface of the structure for elimination. It is the examiner's position that since the cited references, for reasons set forth above and in the previous rejection, teach the same

"special features" that provide the function of stress relief, that the references will inherently and expectedly possess the function of stress relief.

For at least these reasons the rejections set forth in the previous rejection are maintained. Furthermore, in regards to the new claims, new rejections have been set forth.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONATHAN C. LANGMAN whose telephone number is (571)272-4811. The examiner can normally be reached on Mon-Thurs 8:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Callie Shosho can be reached on 571-272-1123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCL
/Jonathan C Langman/
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